CLAIMS

1. A memory cell comprising:

a variable resistor; and

a current controlling device for controlling a current flowing through said variable resistor.

2. A memory cell in accordance with claim 1, wherein said current controlling device is a field-effect transistor.

3. A memory cell in accordance with claim 1, wherein said current controlling device is a diode.

4. A memory cell in accordance with claim 1, wherein said current controlling device is a bipolar transistor.

5. A memory cell in accordance with claim 2, wherein said variable resistor has a resistance body of a perovskite structure.

6. A memory cell in accordance with claim 3, wherein said variable resistor has a resistance body of a perovskite structure.

7. A memory cell in accordance with claim 4, wherein said variable resistor has a resistance body of a perovskite structure.

8. A memory device formed of a plurality of memory cells arranged in a matrix, comprising:

said memory cells, each comprising a variable resistor and a field-effect transistor for controlling a current flowing through said variable resistor;

word lines for connecting the gates of said field-effect transistors in common in the row direction of said matrix;

source drive lines for connecting the sources of said field-effect transistors in common in said row direction; and

bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein

the drains of said field-effect transistors are connected to the other terminals of said variable resistors.

9. A memory device in accordance with claim 8, wherein said word lines are connected to a row decoder for selecting said word lines,

said bit lines are connected to a column decoder for selecting said bit lines, and

a readout circuit is connected to said column decoder to read memory data from said memory cells.

10. A memory device formed of a plurality of memory cells arranged in a matrix, comprising:

said memory cells, each comprising a variable resistor and a

diode for controlling a current flowing through said variable resistor;

word lines for connecting the anodes of said diodes in common in the row direction of said matrix; and

bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein

the cathodes of said diodes are connected to the other terminals of said variable resistors.

11. A memory device in accordance with claim 10, wherein said word lines are connected to a row decoder for selecting said word lines,

said bit lines are connected to a column decoder for selecting said bit lines, and

a readout circuit is connected to said column decoder to read memory data from said memory cells.

12. A memory device formed of a plurality of memory cells arranged in a matrix, comprising:

said memory cells, each comprising a variable resistor and a bipolar transistor for controlling a current flowing through said variable resistor;

a common-connected portion for connecting the collectors of said bipolar transistors in common;

word lines for connecting the bases of said bipolar transistors

in common in the row direction of said matrix;

bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein

the emitters of said bipolar transistors are connected to the other terminals of said variable resistors.

13. A memory device in accordance with claim 12, wherein said word lines are connected to a row decoder for selecting said word lines, said bit lines are connected to a column decoder for selecting said bit lines, and a readout circuit is connected to said column decoder to read memory data from said memory cells.

14. A memory device in accordance with claim 9, wherein said variable resistor has a resistance body of a perovskite structure.

15. A memory device in accordance with claim 11, wherein said variable resistor has a resistance body of a perovskite structure.

16. A memory device in accordance with claim 13, wherein said variable resistor has a resistance body of a perovskite structure.